High Speed and Delay Efficient Convolution by Using Kogge Stone Device

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Abstract – **Various organizations around the world are examining high speed processor for achieving fast digital communication. In this paper, authors propose a method to develop fast convolution technique. Convolution is the bottleneck for digital signal processing, image processing and other signal analysis. With this concern, we need to design a fast multiplier and adder which are also main components of processor design. Calculation of partial products will be handled by Vedic Mathematics named as Urdhva Triyagbhayam sutra. Kogge Stone device for fast speed multiplication and addition has been used in this research. Simulation and synthesis were done on 14.2i Spartan 3 series of Xilinx.**

Keywords: Circular Convolution, Linear Convolution, Kogge Stone Adder (KSA), Vedic Multiplier (VM), Urdhwa

I. INTRODUCTION

WITH the advent of new generation of digital devices, speed of the processor must be high. Processor-speed can be enhanced by the aid of high-speed multiplication and addition of the binary bits. With the latest advancements in VLSI technology, one strives to increase the speed and reduce the area as much as possible. Convolution and de-convolution techniques play an important role in digital signal processing and image processing. Convolution is a mathematical way of combining two signals to form a third signal. On the other hand, deconvolution is the process to calculate the output signal for given input signal by using impulse response signal. Convolution is basically used in digital filter and correlation applications. Convolution can be classified as linear, circular convolution and graphical convolution.

Graphical method is the best way to represent the convolve of two signals but it is quite tedious, so generally we use linear and circular technique in digital signal processing. Computation of convolution depends on multiplier and adder devices. So in this paper, Vedic multiplier based on Urdhva Triyagbhayanm Sutra and Kogge Stone high speed adder is used instead of traditional devices. Multiplication can be done by shifting and adding method but it gives high propagation delay. Another method is Wallace tree algorithm but it is not better than Kogge Stone adder in terms of area.

$$y(n) = f(n) * g(n) \tag{1}$$

where, f(n) and g(n) are finite-length sequences.

$$y(n) = \sum_{n=-\infty}^{+\infty} [f(k) * g(n-k)] \tag{2}$$

Linear Convolution can be calculated by using above equations. But this is lengthy process. This can be solved by several methods: Cross multiplication is one of the best ones.

II. CROSS MULTIPLICATION BY USING VEDIC MATHEMATICS

Vedic mathematic comprises of 16 sutras proposed by Jagadguru Swami Bharathi Krishna Trithaji of Govardhan Peeth, Puri Jaganath (1884-1960). Urdhva Triyagbhayam sutra is applicable for all. Udhva Triyagbhayam sutra is essential technique for fast multiplication which is based on vertically and cross connections [1]. This method is the part and partial technique for low power VLSI design and Digital signal processing. Urdhav Triyagbhayam is a novel concept through which throughput is obtained parallel. Generation of partial products and their summation is obtained using this algorithm which is explained in figure [1]. The special feature that differentiates it from other conventional process is that it reduces the need of resources from process to operate at high frequencies. The striking feature of Vedic multiplier based on Urdhava Triyagbhayam method is that as the number of bits increases, area and gate delay increases at a faded rate as compared to other multipliers. Figure 1 shows the binary cross multiplication by using Udhva Triyagbhayam Vedic multiplication technique.

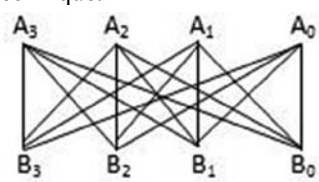

Figure 1: A vedic cross multiplication technique to multiply 4 bit information.

Here (A_3,A_2,A_1,A_0) and (B_3,B_2,B_1,B_0) bits are multiplied together and produce 8 bit output sequence. First, A_0 is vertically multiplied with B_0 that would be the first product bit. It can be designed by using the simple AND gate. For the second product bit A_1 is cross multiplied with B_0 and A_0 is cross multiplied with B_1 then both partial products will be added by using the half adder device. Next product bit can be computed by using vertically and cross multiplication, A_2 is diagonally partial multiplied with B_0, A_0 is cross multiplied with B_2 and A_1 is vertically multiplied with B_1, now these bits can be added by using half-adder and full-adder. In the same manner, other remaining bits can be found. Udhva Triyagbhayam sutra is one of the most efficient techniques of multiplication. By the aid of this technique, number of computing steps can be reduced. Number of gates and elements are dependent on calculation of steps. Further this method can be enhanced for 8 bit, 16 bit and 32 bit parallel adder. So, Vedic mathematic provides the less complexity then other calculation techniques.

III. APPROACHING HIGH SPEED CONVOLUTION METHOD

A. Linear Convolution: Convolution of two discrete finite length signals can be calculated by several techniques and cross multiplication is one of them. By using Vedic mathematics typical calculation can be performed within less time [2]. Let us assume that f(n) is a finite length sequence of (A_3,A_2,A_1,A_0) and another finite length sequence is g(n) with variables (B_3,B_2,B_1,B_0) then output will be y(n) with finite length sequence (Y_6,Y_5,Y_4,Y_3,Y_2,Y_1,Y_0). For instance Input sequences are A(7,7,7,7) and B(7,7,7,7) then linear convolution output will be (49,98,147,196,147,98,49).

$$\begin{aligned} Y_0 &= A_0 * B_0 \\ Y_1 &= A_1 * B_0 + A_0 * B_1 \\ Y_2 &= A_2 * B_0 + A_1 * B_1 + A_0 * B_2 \\ Y3 &= A_0 * B_3 + A_1 * B_2 + A_2 * B_1 + A_3 * B_0 \\ Y4 &= A_1 * B_3 + A_2 * B_2 + A_3 * B_1 \\ Y_5 &= A_2 * B_3 + A_3 * B_2 \\ Y_6 &= A_3 * B_3 \end{aligned} \tag{3}$$

In these equations all the calculation of multiplication will be done by Urdhva Triyagbhayam technique and addition will be performed by Kogge Stone Adder. With the aid of this technique we can reduce the number of gates and area; As numbers of slices are decreased, propagation delay or route delay gets automatically reduced [3].

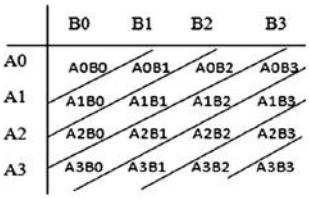

Figure 2: A matrix fast Linear Convolution by using cross Multiplication.

Figure 2 shows, the fast linear convolution by using cross multiplication, here elements of each diagonal line are added together individually. Here bits of A group are put in a vertical way and bits of B group are putted in horizontal way.

Now A_0 is multiplied with B_0 in partial product manner that is also called ANDing Operation. After this partial product, A_0 is multiplied with other remaining bits such as B_1, B_2 and B_3. Likewise A_1 is multiplied with B_0 in partial manner. A_1 is multiplied with B_1 and B_0. In the same manner, other bit will be multiplied with remaining bits. The output will be found by adding of these partial products. Diagonally lines show the addition of the individual outputs. Eventually, convolution of the 4 bit provides the output of the 7 bit. This convolution method can be enhanced for 5, 6 and other bit sequences.

Circular convolution is the most frequently used in filtering the noise and blurred signal in digital signal processing and image signal processing. Circular convolution has many applications and is usually applicable to electrical engineering students in a digital signal processing. A Vedic mathematics multiplication is a novel method for computing the circular convolution [4]. Circular convolution can be obtained by using the shifting and folding technique but it gives complex solution. So in paper we are using Vedic multiplication and Kogge Stone adder to compute the circular convolution sequence. Let us assume that *f(n)* and *g(n)* are finite length sequence then output of circular convolution *y(n)* is

$$y(n) = f(n) * g(n) \tag{4}$$

$$y(n) = \sum_{n=0}^{N-1} [f(k) * g(n-k)(ModN)] \tag{5}$$

where, N is the length of the sequences. for instance one finite Length sequence is (A_3,A_2,A_1,A_0) and another sequence is (B_3,B_2,B_1,B_0) then output sequence for circular convolution is (Y_3,Y_2,Y_1,Y_0).

$$\begin{aligned} Y_0 &= A_0 * B_0 + A_3 + B_1 + A_2 + B_2 + A_1 * B_3 \\ Y_1 &= A_1 * B_0 + A_0 + B_1 + A_3 + B_2 + A_2 * B_3 \\ Y_2 &= A_2 * B_0 + A_1 + B_1 + A_0 + B_2 + A_3 * B_3 \\ Y_3 &= A_3 * B_0 + A_2 + B_1 + A_1 + B_2 + A_0 * B_3 \end{aligned} \tag{6}$$

In circular convolution no carry out will be propagated to other equations.

IV. LOGICAL DESIGNING APPROACH OF HIGH SPEED LINEAR CONVOLUTION

Complex logical designing can be reduced by the Vedic mathematics calculation which is consist with 16 sutras. Number of fan in, fan out pin and input output buffers can be minimized. For the high speed convolution, multiplier and adder must be high efficient and of low area. For instance

(A_3,A_2,A_1,A_0) and (B_3,B_2,B_1,B_0) are the finite length sequence. In the linear convolution total number of Vedic multiplier will be 16 for 4 bit multiplication. Each Vedic multiplier produce 8 bit output summation bits. So we need 8 bit adder for adding the two 8 bit sequence which is performed by low propagation delay Kogge Stone adder [6]. 8 bit Kogge Stone Adder produces the 9 bit output. These bits are added by 9 bit Kogge Stone Adder which produces 10 bit output bit sequence. Hence total number of output bit for 4-bit high-speed liner convolution is 64 use the 4 bit Vedic multiplier, 8 and 9 bit Kogge Stone adder. Multiplication of convolution input sequence is different from ordinary binary multiplication [5]. In the multiplication of convolution input sequence no carry forward to next bit or addition will be performed individually. With other instance this technique can be made understood easily. If input sequence of convolution are (15,15,15,15) and (15,15,15,15) then output sequence will be (225,450,675,900,675,450,225). So, maximum output bits are 64 of 4 high bit sequence. Here we are using 4 high bit for 4 input sequence so total number of bit for A input sequence are 16, like for B input sequence.

Figure 3 shows the 4-bit high efficient linear convolution logic design. Here, number of inputs are 16. And first 4 bits are multiplied by using the 4 bit high speed Vedic multiplier which is abbreviated by VM. The output of the first Vedic multiplier gives the 8-bit output that is the first 8 bit output of the linear convolution. Now the next 4-bit Vedic multiplier multiplies the different 4-bit inputs and outputs are connected to the 8-bit adder. This is special high speed Kogge Stone adder which provides the low combinational delay with less area. Third multiplier multiplies the 4-bit of a [7:3] and b [3:0] and this gives the 8-bit outputs. These output bits are connected to the 8 bit Kogge Stone adder. So output bits of the second Vedic multiplier and output bits of third Vedic multiplier are connected to inputs of the 8 bit KSA. This adder provides the 9 bit output of the linear convolution and sequence would be P [16:8]. Same as previous step the output bits of the forth and fifth Vedic multiplier are added by 8 bit KSA. And output bits of the 8 bit KSA are connected to the 9 bit Kogge Stone adder. The Kogge Stone adder has one special property is that its propagation delay does not depend on the increased logic circuit. So propagation delay of the 8 ,9 10 and other than this are having same propagation delay.

Vedic multiplier of the sixth number provides the 8 bit output and these bits are connected to the 9 bit KSA. So output of the second 8 bit KSA and output of the sixth Vedic multiplier are added by 9 bit KSA. This 9 bit Kogge Stone adder gives the 10 bit of the linear convolution that is P [26:17]. To find the next output of the convolution P [36:27] two 8 bit KSA and one 9 bit KSA are needed. Likewise the output P [46:37] can be found by using the one 8 bit KSA and 9 bit KSA is required. Next output bits P[55:47] can be found by using the only one 8 bit KSA. The last group of the output P[63:56] can be found directly without adder. The concept of the linear convolution is just like as the simple multiplication of the binary bit but difference is that the carry bit will not be forwarded to the next bit.

KS adder: Input sequence of Conventional method is much more than the proposed method, however proposed method has less propagation delay. Area and propagation delay can be reduced by the aid of proposed kogge stone (KS) adder. This adder will be designed like as ripple carry adder. Carry output of one KS adder is connected with another KS adder but this method is very beneficiary for high efficient digital devices as per concerning propagation delay.

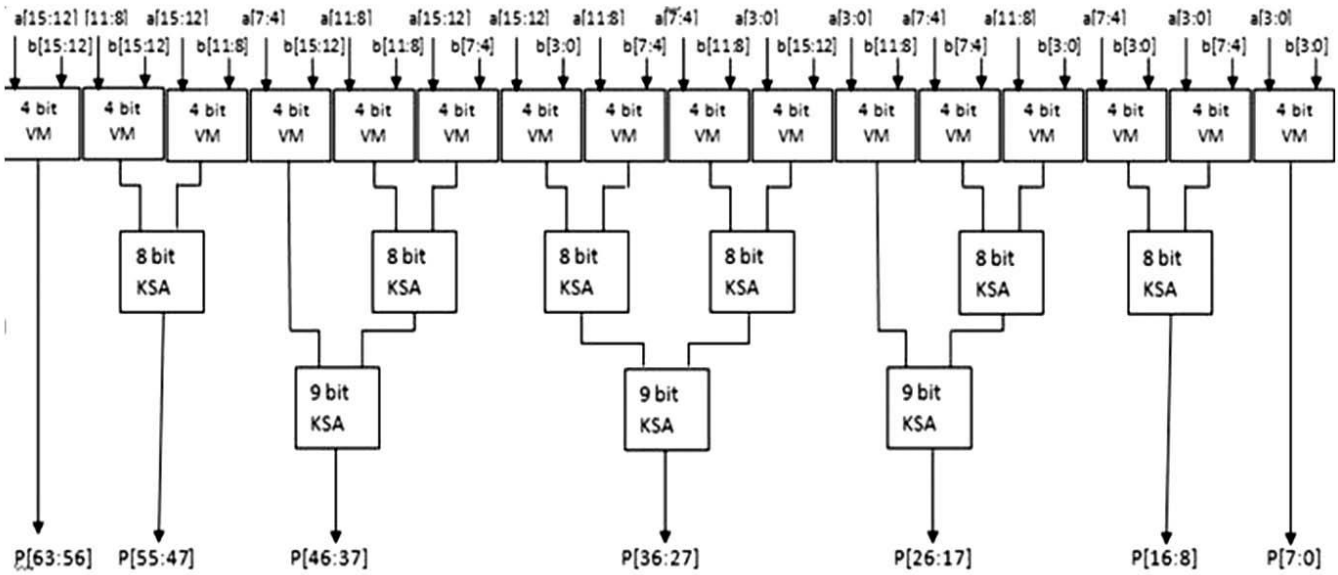

Figure 3. A 4-bit High Speed Linear Convolution.

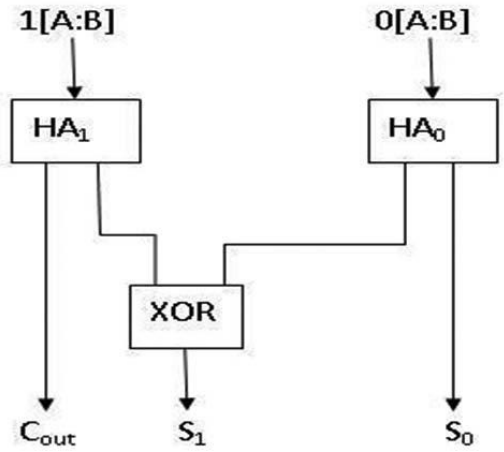

Figure 4. A proposed 2 bit KS Adder.

V. EXPERIMENTAL SETUP

All the experiment analysis is done by 14.2i Spartan 3 series Xilinx tool. This tool provides less propagation delay than the 6.2i and 9.2i Xilinx tool. The most important advantage of this tool is less memory with high speed analysis any complex logical circuit. Simulation and synthesize of convolution logical circuit can be enhanced by Xilinx design suit 14.2i Spartan 3 series and device XC3S400-5fg320.

VI. COMPARISON OF MODIFIED METHOD WITH CONVENTIONAL METHOD

Proposed high speed convolution via Vedic multiplier and Kogge Stone can be compared with conventional method which is computed by Vedic multiplier, full adder and half adder [7]. Proposed technique provides less path delay and less area. Input sequence of Conventional method is much more than to proposed method, however proposed method has less propagation delay.

TABLE 1 – COMPARISON BETWEEN CONVENTIONAL ADDER AND PROPOSED ADDER

7 i/p Sequence				
	Slices	LUTs	IOBs	MCPD
Sign multiplier with parallel adder	276 out of 768	498 out of 1536	76 out of 124	22.345 ns
Sign multiplier with conventional adder	234 out of 768	408 out of 1536	76 out of 124	20.090 ns
Sign multiplier with proposed adder	222 out of 768	384 out of 1536	76 out of 124	19.294 ns

TABLE 2 – COMPARISON BETWEEN CONVENTIONAL ADDER AND PROPOSED ADDER

9 i/p Sequence				
	Slices	LUTs	IOBs	MCPD
Sign multiplier with parallel adder	726 out of 768	1266 out of 1536	125 out of 124	35.789 ns
Sign multiplier with conventional adder	404 out of 768	705 out of 1536	100 out of 124	21.356 ns
Sign multiplier with proposed adder	393 out of 768	689 out of 1536	100 out of 124	19.989 ns

Table 3 shows comparison of the conventional and modified high-speed convolution technique. The parameters are input, output sequence, slices, input output buffers, and look up table and propagation delay that is also called combinational path delay. According to this table, input sequence is [3:0] that is 4 bit sequences.

TABLE 3 – COMPARISON BETWEEN PREVIOUS ALGORITHM AND PROPOSED ALGORITHM

Parameter	**Conventional method**	**Proposed method**
Elements used	Array Multiplier, HA and FA	Vedic Multiplier and KS Device
I/P sequence	A[3 :0] and B[3:0]	A[3 :0] and B[3 : 0]
No of slices	358	222
No of IO Buffers	96	76
No of LUTs	623	384
Propagation Delay	21.963 ns	19.989 ns

Number of slices of the conventional method is less than the modified convolution technique. Number of the input, outputs buffers is having same value for both. The main motive of this paper is to reduce the propagation delay. Propagation delay is an essential parameter to design the high speed convolution technique.

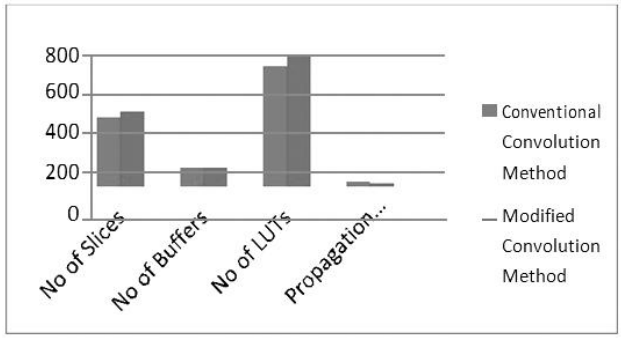

Figure 5. Graph depicting comparison between Conventional and Modified Linear Convolution Technique.

Above graph shows the parameter comparison between conventional and modified 4-bit linear high-speed convolution technique. The number of slices and LUTs are more but propagation delay is less. Main object of the paper is to reduce the propagation delay. Propagation delay or combinational path delay is a crucial parameter vis-a-vis others.

VII. CONCLUSION

A fast linear convolution circuit based on Vedic multiplier and Kogge Stone adder is examined. The path delay time and area of the proposed technique for convolution using Vedic multiplication algorithm as compared with that of convolution with simple multiplication is less. Regarding the propagation delay, simple Vedic multiplication using linear convolution: it is 45% more than the convolution using the Vedic multiplication as well as Kogge Stone adder.

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